RTL8188ER-CG

SINGLE-CHIP IEEE 802.11b/g/n 1T1R WLAN

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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Realtek Semiconductor Corp.
No. 2, Innovation Road II, Hsinchu Science Park, Hsinchu 300, Taiwan
Tel.: +886-3-578-0211. Fax: +886-3-577-6047
www.realtek.com

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2012/01/30	Preliminary release
0.2	2012/04/19	Correct ordering information
0.3	2012/5/22	Modify Fig 1, 2, 3

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek RTL8188ER is a highly integrated single-chip 802.11n Wireless LAN (WLAN) network PCIe interface (PCIe 1.0/1.0a/1.1 compliant) controller. It combines a WLAN MAC, a 1T1R capable WLAN baseband, and WLAN RF in a single chip. The RTL8188ER provides a complete solution for a high throughput performance integrated wireless LAN device.

The RTL8188ER WLAN baseband implements Orthogonal Frequency Division Multiplexing (OFDM) with 1 transmit and 1 receive path and is compatible with the IEEE 802.11n specification. Features include one spatial stream transmission, short guard interval (GI) of 400ns, spatial spreading, and transmission over 20MHz and 40MHz bandwidth.

For legacy compatibility, Direct Sequence Spread Spectrum (DSSS), Complementary Code Keying (CCK) and OFDM baseband processing are included to support all IEEE 802.11b and 802.11g data rates. Differential phase shift keying modulation schemes, DBPSK and DQPSK with data scrambling capability, are available, and CCK provides support for legacy data rates, with long or short preamble. The high-speed FFT/IFFT paths, combined with BPSK, QPSK, 16QAM, and 64QAM modulation of the individual subcarriers and rate compatible punctured convolutional coding with coding rate of 1/2, 2/3, 3/4, and 5/6, provide higher data rates of 54Mbps and 150Mbps for IEEE 802.11g and 802.11n OFDM respectively.

The RTL8188ER WLAN Controller builds in an enhanced signal detector, an adaptive frequency domain equalizer, and a soft-decision Viterbi decoder to alleviate severe multi-path effects and mutual interference in the reception of multiple streams.

Efficient IQ-imbalance, DC offset, phase noise, frequency offset, and timing offset compensations are provided for the radio frequency front-end. Selectable digital transmit and receive FIR filters are provided to meet transmit spectrum mask requirements and to reject adjacent channel interference, respectively.

The RTL8188ER WLAN Controller supports fast receiver Automatic Gain Control (AGC) with synchronous and asynchronous control loops among antennas, antenna diversity functions, and adaptive transmit power control function to obtain the better performance in the analog portions of the transceiver.

The RTL8188ER WLAN MAC supports 802.11e for multimedia applications, 802.11i for security, and 802.11n for enhanced MAC protocol efficiency. Using packet aggregation techniques such as A-MPDU

with BA and A-MSDU, protocol efficiency is significantly improved. Power saving mechanisms such as Legacy Power Save, and U-APSD, reduce the power wasted during idle time, and compensates for the extra power required to transmit OFDM. The RTL8188ER provides simple legacy and 20MHz/40MHz co-existence mechanisms to ensure backward and network compatibility.

2. Features

General

- 56-pin QFN
- CMOS MAC, Baseband PHY, and RF in a single chip for IEEE 802.11b/g/n compatible WLAN
- Complete 802.11n solution for 2.4GHz band
- 72.2Mbps receive PHY rate and 72.2Mbps transmit PHY rate using 20MHz bandwidth
- 150Mbps receive PHY rate and 150Mbps transmit PHY rate using 40MHz bandwidth
- Compatible with 802.11n specification
- Backward compatible with 802.11b/g devices while operating in 802.11n mode

Interface

- Complies with PCIe 1.0/1.0a/1.1 for WLAN

Standards Supported

- IEEE 802.11b/g/n compatible WLAN
- IEEE 802.11e QoS Enhancement (WMM)
- 802.11i (WPA, WPA2). Open, shared key, and pair-wise key authentication services

WLAN MAC Features

- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth

WLAN PHY Features

- IEEE 802.11n OFDM
- One Transmit and one Receive path (1T1R)
- 20MHz and 40MHz bandwidth transmission
- Short Guard Interval (400ns)
- DSSS with DBPSK and DQPSK, CCK modulation with long and short preamble
- OFDM with BPSK, QPSK, 16QAM, and 64QAM modulation.
  Convolutional Coding Rate: 1/2, 2/3, 3/4, and 5/6
- Maximum data rate 54Mbps in 802.11g and 150Mbps in 802.11n
- Switch diversity for DSSS/CCK
- Hardware antenna diversity in per packet base
- Selectable receiver FIR filters
- Programmable scaling in transmitter and receiver to trade quantization noise against increased probability of clipping
- Fast receiver Automatic Gain Control (AGC)
- On-chip ADC and DAC

Peripheral Interfaces

- General Purpose Input/Output (8 pins)

- Three configurable LED pins

3. Application Diagram

3.1. Single-Band 11n (1x1) Solution with Single Antenna

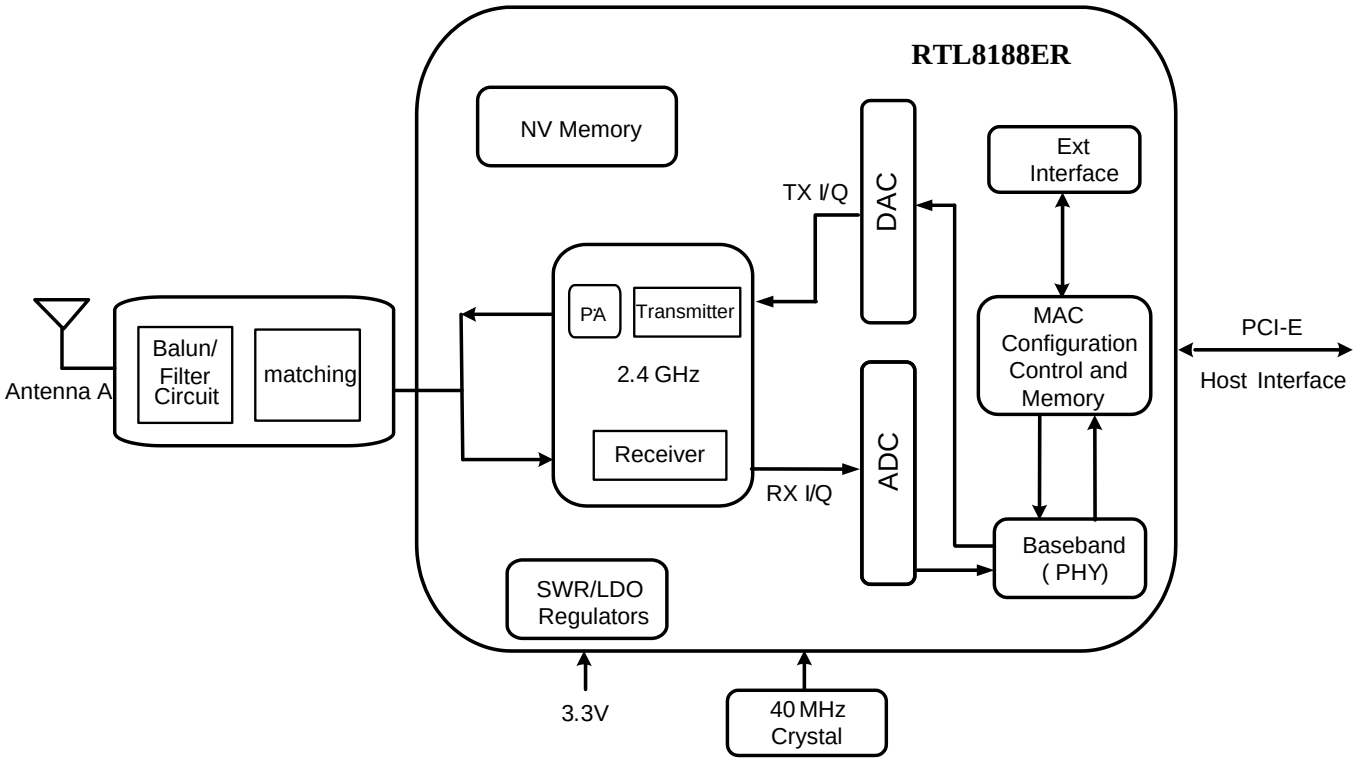


Figure 1. Single-Band 11n (1x1) Solution

3.2. Single-Band 11n (1x1) Solution with Transmit & Receive Diversity

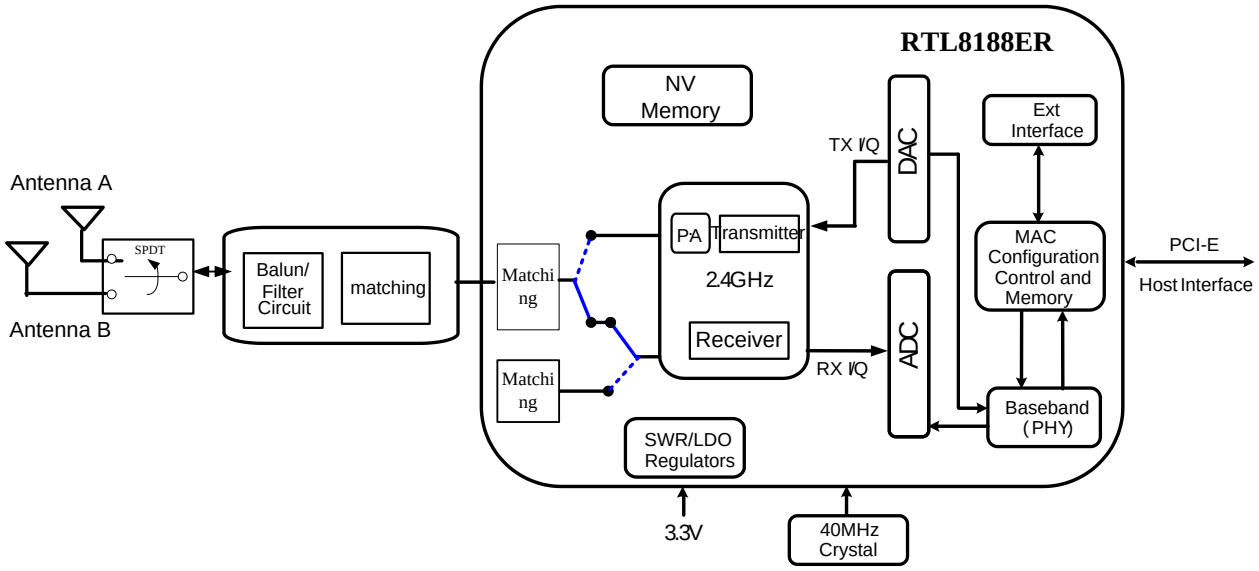


Figure 2.Single-Band 11n (1x1) dual antenna diversity Solution

3.3. Single-Band 11n (1x1) Solution with Receive-Only Diversity

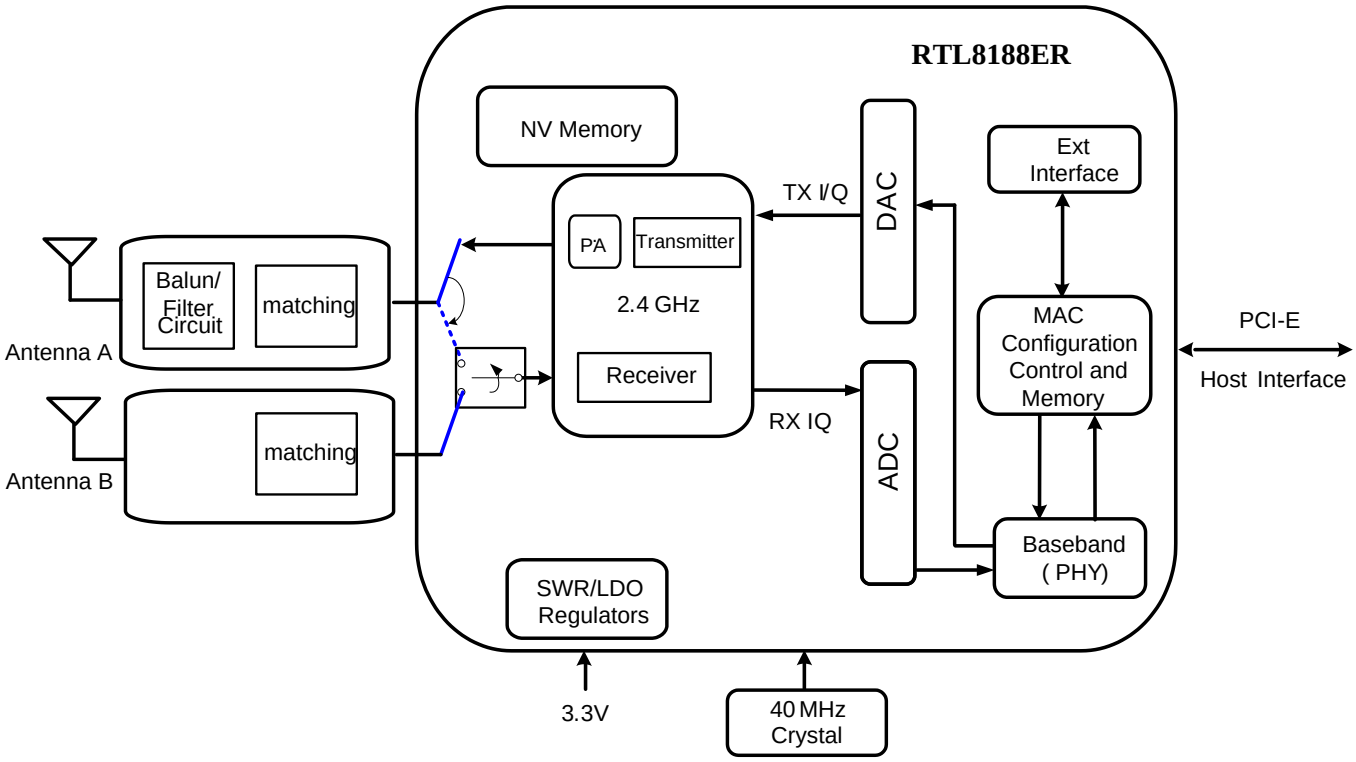


Figure 3. Single-Band 11n (1x1) dual antenna Solution

4. Pin Assignments

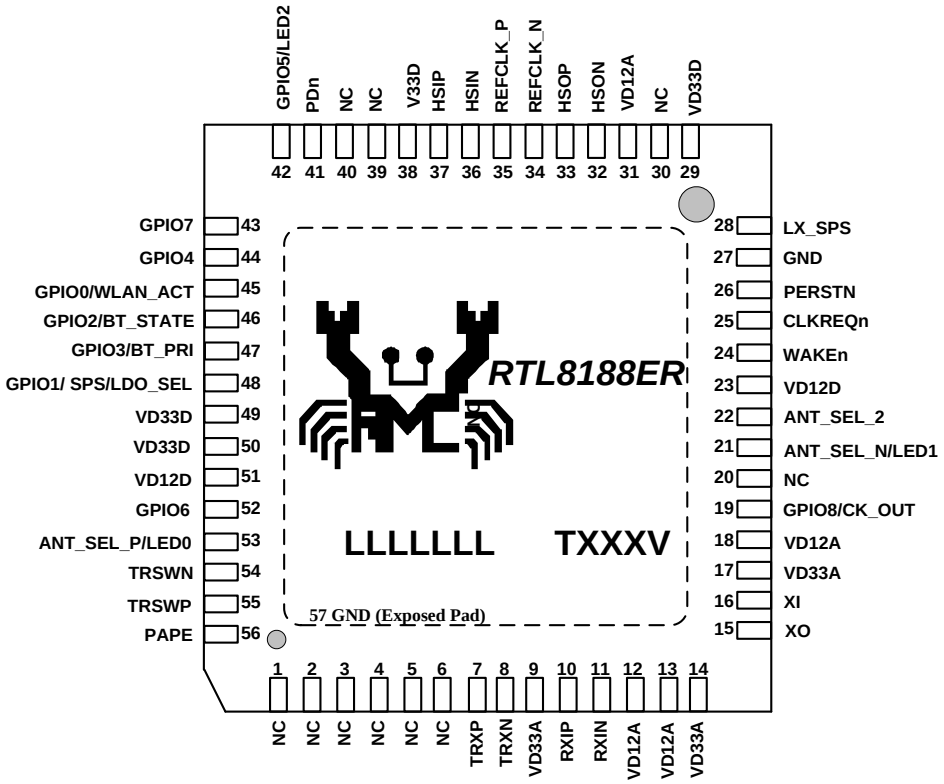


Figure 4. Pin Assignments

4.1. Package Identification

'Green' package is indicated by a 'G' in the location marked 'T' in Figure 4.

5. Pin Descriptions

The following signal type codes are used in the tables:

I: Input	O: Output
T/S: Tri-State bi-directional input/output pin	S/T/S: Sustained Tri-State

O/D: Open Drain P: Power pin

5.1. PCI Express Transceiver Interface

Table 1. PCI Express Transceiver Interface

Symbol	Type	Pin No	Description
HSIN/HSIP	I	36/37	PCI Express Receive Differential Pair
HSON/HSOP	O	32/33	PCI Express Transmit Differential Pair
REFCLK_N/REFCLK_P	I	34/35	PCI Express Differential Reference Clock Source: 100MHz ± 300ppm
CLKREQn	O	25	Reference Clock Request Signal This signal is used by the RTL8188CE-GR to request starting of the PCI Express reference clock
WAKEn	O/D	24	Power Management Event: Open drain, active low Used to reactivate the PCI Express slot's main power rails and reference clocks.
PERSTn	I	26	PCI Express Reset Signal: Active low When the PERSTB is asserted at power-on state, the RTL8188CE-GR returns to a pre-defined reset state and is ready for initialization and configuration after the de-assertion of the PERSTB.

5.2. Power Pins

Table 2. Power Pins

Symbol	Type	Pin No	Description
LX_SPS	P	28	Switching Regulator Output
VD33A	P	9,14,17	VDD 3.3V for Analog
VD33D	P	29,38,49,50	VDD 3.3V for Digital
VD12A	P	12,13,18,31	Analog 1.2V Input
VD12D	P	23,51	Digital 1.2V Input
GND	P	27,57	Ground

5.3. RF Interface

Table 3. RF Interface

Symbol	Type	Pin No	Description
TRSWN	O	54	Transmit/Receive Shared with LED2, can be selected by control register
PAPE	O	56	2.4GHz Transmit Power Amplifier Power Enable 0
TRSWP	O	55	Transmit/Receive Signal
TRXP	O	7	RF TX Negative Signal

Symbol	Type	Pin No	Description
TRXN	O	8	RF TX Positive Signal
RX_IP	I	10	RF RX Positive Signal
RX_IN	I	11	RF RX Negative Signal
ANT_SEL_P	O	53	Antenna Control Positive Signal Shared with LED0, can be selected by control register
ANT_SEL_N	O	21	Antenna Control Negative Signal Shared with LED1, can be selected by control register
ANT_SEL_2	O	22	Antenna Control Extend Signal

5.4. LED Interface

Table 4. LED Interface

Symbol	Type	Pin No	Description
LED0	O	53	LED Pins (Active Low) Shared with ANT_SEL_P, can be selected by control register
LED1	O	21	LED Pins (Active Low) Shared with ANT_SEL_N, can be selected by control register
LED2	O	42	LED Pins (Active Low) Shared with GPIO5, can be selected by control register

5.5. Clock and Other Pins

Table 5. Clock and Other Pins

Symbol	Type	Pin No	Description
XI	I	16	40MHz OSC Input Input of 40MHz Crystal clock reference
XO	O	15	Output of 40MHz Crystal Clock Reference
PDn	I	41	This Pin can Externally Shutdown RTL8188ER without Extra Power Switch
GPIO0/WLAN_ACT	IO	45	General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_ACT Pin The WLAN_ACT signal indicates when WLAN is either transmitting or receiving in the 2.4GHz ISM band.
GPIO1/ (SPS/LDO_SEL)	IO	48	Trap Function: Decide to use the SWR or LDO for 3.3V -> 1.2V by this pin power on latch low or high. LDO_SPS_SEL = 0, use SWR LDO_SPS_SEL = 1, use LDO General Purpose Input/Output Pin or Bluetooth Coexistence WLAN_RX Pin.
GPIO2/BT_STATE	IO	46	General Purpose Input/Output Pin or Bluetooth Coexistence BT_STAT Pin The BTSTAT signal indicates when normal Bluetooth packets are being transmitted or received.
GPIO3/BT_PRI	IO	47	General Purpose Input/Output Pin or Bluetooth Coexistence BT_PRI Pin The BTPRI signal indicates when a high priority Bluetooth packet is being transmitted or received.
GPIO4	IO	44	General Purpose Input/Output Pin
GPIO5/LED2	IO	42	General Purpose Input/Output Pin Shared with LED2, can be selected by control register
GPIO6	IO	52	General Purpose Input/Output Pin. If the GPIO is not used, please leve it open.
GPIO7	IO	43	This pin can also support WLAN Radio off function with host interface remaining connected.
GPIO8/CK_OUT	O	19	General Purpose Input/Output Pin Buffered 40M clock outputs for other peripheral IC

6. Electrical and Thermal Characteristics

6.1. Temperature Limit Ratings

Table 6. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	0	70	°C
Junction Temperature	0	125	°C

6.2. Thermal Parameters

Table 7. Thermal Parameters

Parameter	SYM	Condition	Air Flow 0 m/s	Units
Thermal Resistance: Junction to ambient	θja	2-layer FR4 PCB	31.7	°C/W
Thermal Characterization: Junction to Case	θjc	2-layer FR4 PCB	13.4	°C/W

Note: PCB conditions (JEDEC JESD51-7). Dimensions: 76.2mm x 114 mm. Thickness: 1.6mm.

6.3. DC Characteristics

6.3.1. Power Supply Characteristics

Table 8. DC Characteristics

Symbol	Parameter	Minimum	Typical	Maximum	Units
VD33A, VD33D	3.3V I/O Supply Voltage	3.0	3.3	3.6	V
VD12A, VD12D	1.2V Core Supply Voltage	1.10	1.2	1.32	V
VD15A, VD15D	1.5V Supply Voltage	1.425	1.5	1.575	V
IDD33	3.3V Rating Current	-	-	600	mA

6.3.2. Digital IO Pin DC Characteristics

Table 9. 3.3V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	2.0	3.3	3.6	V
V_{IL}	Input low voltage	--	0	0.9	V
V_{OH}	Output high voltage	2.97	--	3.3	V
V_{OL}	Output low voltage	0	--	0.33	V

Table 10. 2.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.8	2.8	3.1	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	2.5	--	3.1	V
V_{OL}	Output low voltage	0	--	0.28	V

Table 11. 1.8V GPIO DC Characteristics

Symbol	Parameter	Minimum	Normal	Maximum	Units
V_{IH}	Input high voltage	1.7	1.8	2.0	V
V_{IL}	Input low voltage	--	0	0.8	V
V_{OH}	Output high voltage	1.62	--	1.8	V
V_{OL}	Output low voltage	0	--	0.18	V

7. Interface Timing Specification

7.1. PCIe Bus during Power On Sequence

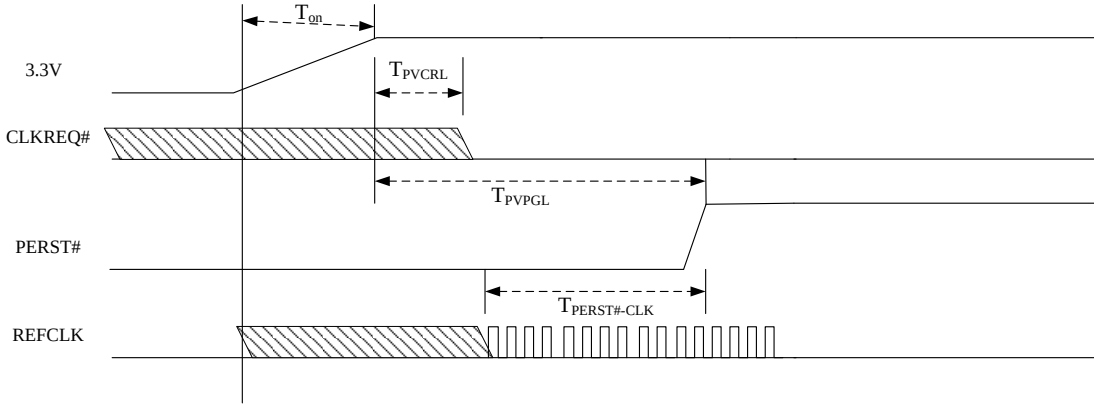


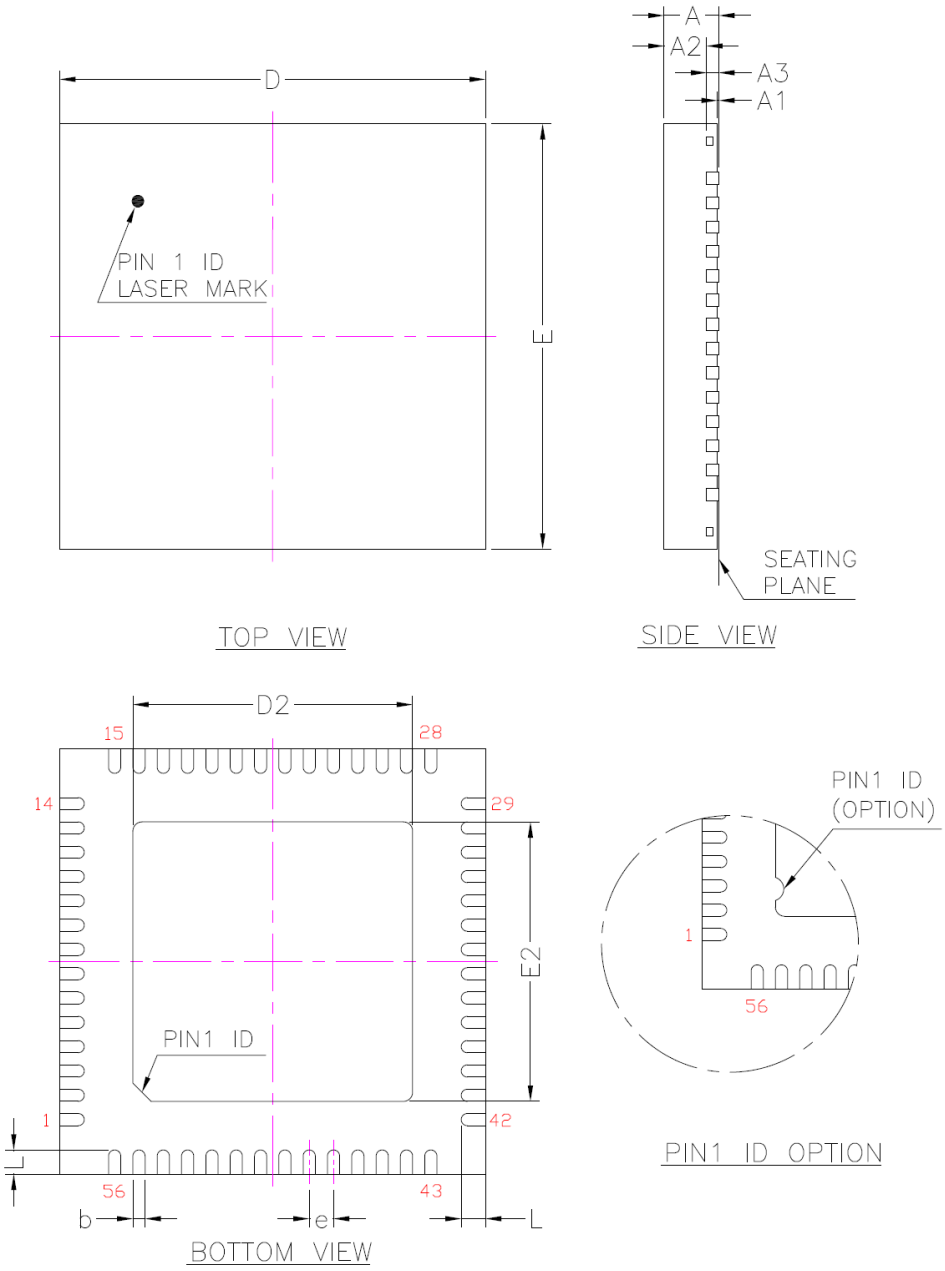
Figure 5. RTL8188ER PCIe Bus Power On Sequence

T_{on}: The main power ramp up duration
T_{PVCRL}: Power valid to CLKREQ# output active
T_{PVPGL}: Power valid to PERST# input inactive
$T_{PERST\#-CLK}$: Reference clock stable before PERST# inactive

Table 12. The typical timing range

symbol	Unit	Min	Typical	Max
T_{on}	ms	--	1.5	5
T_{PVCRL}	us	--		100
T_{PVPGL}	ms	1		--
$T_{PERST\#-CLK}$	us	100		--

8. Mechanical Dimensions



8.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	0.80	0.85	0.90	0.031	0.033	0.035
A_1	0.00	0.02	0.05	0.000	0.001	0.002
A_2	---	0.65	0.70	---	0.026	0.028
A_3	0.2 REF			0.008 REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E	7.00 BSC			0.276 BSC		
D_2/E_2	4.35	4.60	4.85	0.171	0.181	0.191
e	0.40 BSC			0.016 BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MO-220.

9. Ordering Information

Table 13. Ordering Information

Part Number	Package	Status
RTL8188ER-CG	QFN-56, 'Green' Package	Mass Production

Note: See page 7 for package identification.

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Hsinchu Science Park,
Hsinchu 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com